CLAIMS

1. A capacitive structure, comprising:

a semiconductor base region having an upper surface;

a well formed within the semiconductor base region and adjacent the upper surface;

a first dielectric layer adjacent at least a portion of the upper surface;

a polysilicon layer adjacent the first dielectric layer, wherein the well, the first dielectric layer, and the first polysilicon layer form a first capacitor and are aligned along a planar dimension;

a first conductive layer positioned with at least a portion overlying at least a portion of the polysilicon layer;

a second dielectric layer adjacent the first conductive layer; and

a second conductive layer adjacent the second dielectric layer, wherein the first conductive layer, the second dielectric layer, and the second conductive layer form a second capacitor and are aligned along the planar dimension.

2. The capacitive structure of claim 1 and further comprising an electrical connection between the polysilicon layer and the first conductive layer.

3. The capacitive structure of claim 2:

wherein the first conductive layer has a first side adjacent the second dielectric layer and a second side facing in a direction toward the upper surface; and

wherein the electrical connection contacts the second side of the first conductive layer.

4. The capacitive structure of claim 3 wherein the electrical connection is substantially perpendicular to the planar dimension.

5. The capacitive structure of claim 2 wherein the electrical connection comprises a first electrical connection, and further comprising a second electrical connection between the second conductive layer and the well.

6. The capacitive structure of claim 5:

wherein the well comprises a length having a first end and a second end;

wherein the second electrical connection is between the second conductive layer and the first end of the well; and

wherein the second end of the well is for connecting to a fixed potential.

7. The capacitive structure of claim 6 wherein the fixed potential is ground.

8. The capacitive structure of claim 6:

wherein the fixed potential equals a first fixed potential; and

wherein the first electrical connection is for connecting to a second fixed potential that is unequal to the first fixed potential.

9. The capacitive structure of claim 5 wherein the second electrical connection comprises:

a first metal layer comprising a first region and a second region electrically separate from the first region, wherein the first region is adjacent the second conductive layer;

a second metal layer at a distance grater than a distance between the upper surface and the first region of the first metal layer;

an electrical connection between the first region of the first metal layer and the second metal layer;

an electrical connection between the second metal layer and the second region of the first metal layer; and

an electrical connection between the second region of the first metal layer and the well.

10. The capacitive structure of claim 9:

wherein the second conductive layer has a first length in a first dimension along the planar dimension and a first width in a second dimension along the planar dimension that is perpendicular to the first length;

wherein the first region of the first metal layer has a second length, less than the first length, and in the first dimension; and

wherein the first region of the first metal layer has a second width, less than the first width, and in the second dimension.

11. The capacitive structure of claim 10 wherein the first conductive layer and the second conductive layer comprise TaN.

12. The capacitive structure of claim 10 wherein the second dielectric comprises Ta_2O_5.

13. The capacitive structure of claim 10:

wherein the first conductive layer and the second conductive layer comprise TaN; and

wherein the second dielectric comprises Ta_2O_5.

14. The capacitive structure of claim 10 wherein the second dielectric comprises a dielectric constant greater than 4.0.

15. The capacitive structure of claim 10 wherein the second capacitor has a capacitance greater than a capacitance of the second capacitor.

16. The capacitive structure of claim 1 wherein the semiconductor base region is selected from a set consisting of a semiconductor well and a semiconductor substrate.

17. The capacitive structure of claim 1:

wherein the second conductive layer has a first length in a first dimension along the planar dimension and a first width in a second dimension along the planar dimension that is perpendicular to the first length;

wherein the first region of the first metal layer has a second length, less than the first length, and in the first dimension; and

wherein the first region of the first metal layer has a second width, less than the first width, and in the second dimension.

18. The capacitive structure of claim 1 wherein the first conductive layer and the second conductive layer comprise TaN.

19. The capacitive structure of claim 1 wherein the second dielectric comprises Ta_2O_5.

20. The capacitive structure of claim 1:

wherein the first conductive layer and the second conductive layer comprise TaN; and

wherein the second dielectric comprises Ta_2O_5.

21. The capacitive structure of claim 1 wherein the second dielectric comprises a dielectric constant greater than 4.0.

22. The capacitive structure of claim 21 wherein the second capacitor has a capacitance greater than a capacitance of the second capacitor.

23. A capacitive structure, comprising:

a first capacitor comprising:

a first capacitor plate comprising polysilicon;

a second capacitor plate comprising a semiconductor well; and

a dielectric between the first capacitor plate and the second capacitor plate;

a second capacitor comprising:

a third capacitor plate comprising a conductor;

a fourth capacitor plate comprising a conductor; and

a dielectric between the third capacitor plate and the fourth capacitor plate; and

an electrical connection between the third capacitor plate and the first capacitor plate.

24. The capacitive structure of claim 23 wherein the third capacitor plate and the fourth capacitor plate comprise TaN.

25. The capacitive structure of claim 23 wherein the dielectric between the third capacitor plate and the fourth capacitor plate comprises a material having a dielectric constant greater than 4.0.

26. The capacitive structure of claim 23 wherein the dielectric between the third capacitor plate and the fourth capacitor plate comprises Ta_2O_5.

27. The capacitive structure of claim 23:

wherein the first capacitor is a fixed position relative to a semiconductor substrate; and

wherein the second capacitor is in a fixed position that at least partially overlies the first capacitor.

28. The capacitive structure of claim 27 wherein the electrical connection contacts a surface of the third capacitor plate that faces the semiconductor substrate.

29. The capacitive structure of claim 27 wherein the electrical connection comprises a first electrical connection, and further comprising a second electrical connection between the fourth capacitor plate and the semiconductor well.

30. The capacitive structure of claim 29:

wherein the well has a first end and a second end;

wherein the second electrical connection is between the fourth capacitor plate and the first end of the semiconductor well; and

wherein the second end of the semiconductor well is for connecting to a first fixed potential.

31. The capacitive structure of claim 29 wherein the first electrical connection is for providing a second fixed potential that is unequal to the first fixed potential.

32. A method of forming a capacitive structure, comprising:

first, forming a first capacitor by the steps of:

forming a first capacitor plate comprising polysilicon;

forming a second capacitor plate comprising a semiconductor well; and

forming a dielectric between the first capacitor plate and the second capacitor plate;

second, forming a second capacitor by the steps of:

forming a third capacitor plate comprising a conductor;

forming a fourth capacitor plate comprising a conductor; and

forming a dielectric between the third capacitor plate and the fourth capacitor plate; and

forming an electrical connection between the third capacitor plate and the first capacitor plate.

33. The method of claim 32 wherein the step of forming a second capacitor plate comprising polysilicon further comprises forming a gate region for a transistor proximate the capacitive structure.

34. The method of claim 32 wherein the step of forming a dielectric between the first capacitor plate and the second capacitor plate further comprises forming a gate insulator for a transistor proximate the capacitive structure.

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